

# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060A – JANUARY 1995 – REVISED DECEMBER 1995

## features

- Four 8-Bit D/A Converters
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trim Required
- Single Supply Operation Possible
- CMOS Technology

## applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters e.g., Gain/Offset

## description

The TLC7226C and TLC7226I consist of four 8-bit voltage-output digital-to-analog converters (DACs) with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible (5 V) input port. Control inputs A0 and A1 determine which DAC is loaded when  $\overline{WR}$  goes low. The control logic is speed compatible with most 8-bit microprocessors. Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between them is inherent.

Each DAC includes an output buffer amplifier capable of sourcing up to 5 mA of output current.

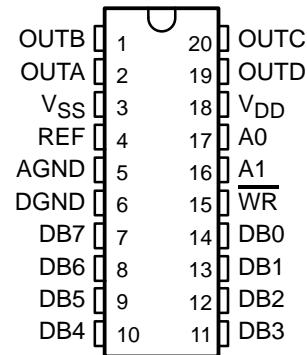
The TLC7226 performance is specified for input reference voltages from 2 V to 12.5 V with dual supplies. The voltage mode configuration of the DACs allows the TLC7226 to be operated from a single power supply rail at a reference of 10 V.

The TLC7226 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7226 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four DACs, four operational amplifiers, and interface logic into either a 0.3-inch wide, 20-terminal DIP or a small 20-terminal small-outline IC (SOIC) allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The pinout is aimed at optimizing board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

The TLC7226C is characterized for operation from 0°C to 70°C. The TLC7226I is characterized for operation from –25°C to 85°C.

DW OR N PACKAGE  
(TOP VIEW)



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 **TEXAS  
INSTRUMENTS**

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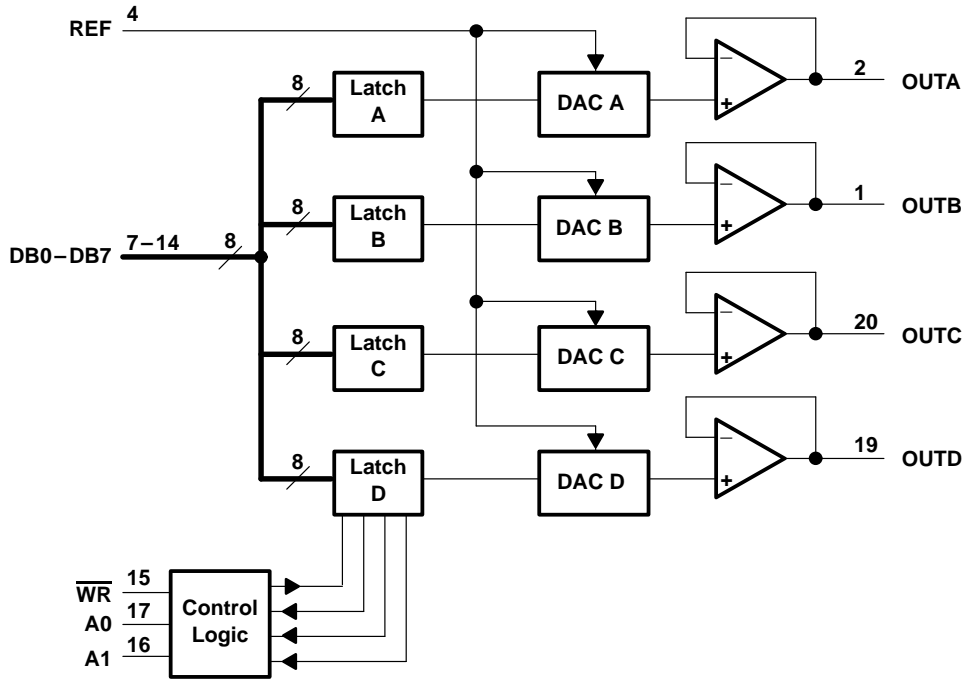
# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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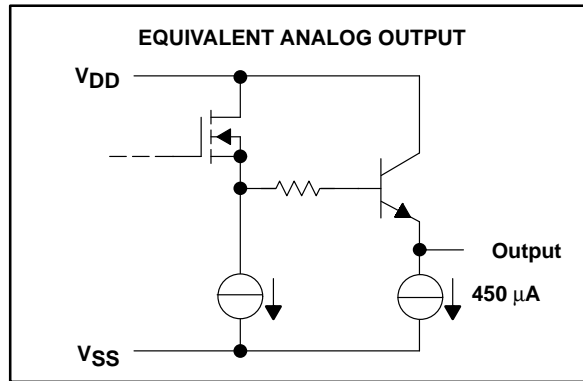
## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC7226CDW	TLC7226CN
-25°C to 85°C	TLC7226IDW	TLC7226IN

## functional block diagram



## schematic of outputs



# TLC7226C, TLC7226I

## QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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### Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
AGND	5		Analog ground
A0, A1	16, 17	I	DAC select inputs
DGND	6		Digital ground
DB0–DB7	7–14	I	Digital DAC data inputs
OUTA	2	O	DACA output
OUTB	1	O	DACB output
OUTC	20	O	DACC output
OUTD	19	O	DACD output
REF	4	I	Voltage reference input
VDD	18		Positive supply voltage
VSS	3		Negative supply voltage
$\overline{WR}$	15	I	Write input selects DAC transparency or latch mode. The selected input latch is transparent when $\overline{WR}$ is low.

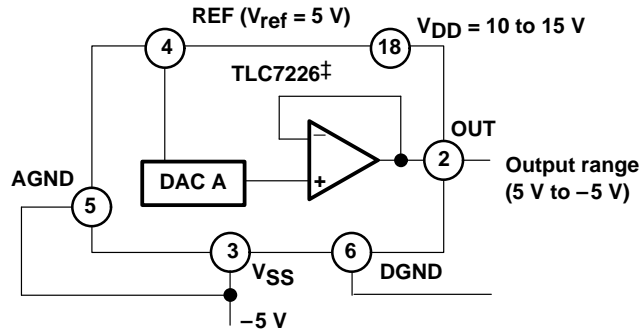
† Terminal numbers shown are for the DW and N packages.

### detailed description

The following sections contain a detailed description of the TLC7226.

#### AGND bias for direct bipolar output operation

The TLC7226 can be used in bipolar operation without adding more external operational amplifiers as shown in Figure 1 by biasing AGND to VSS. This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 1.



‡ Digital inputs omitted for clarity.

**Figure 1. AGND Bias for Direct Bipolar Operation**

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## AGND bias for direct bipolar output operation (continued)

Table 1. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{ref} \left( \frac{127}{128} \right)$
1000	0001	$+V_{ref} \left( \frac{1}{128} \right)$
1000	0000	0 V
0111	1111	$-V_{ref} \left( \frac{1}{128} \right)$
0000	0001	$-V_{ref} \left( \frac{127}{128} \right)$
0000	0000	$-V_{ref} \left( \frac{128}{128} \right) = -V_{ref}$

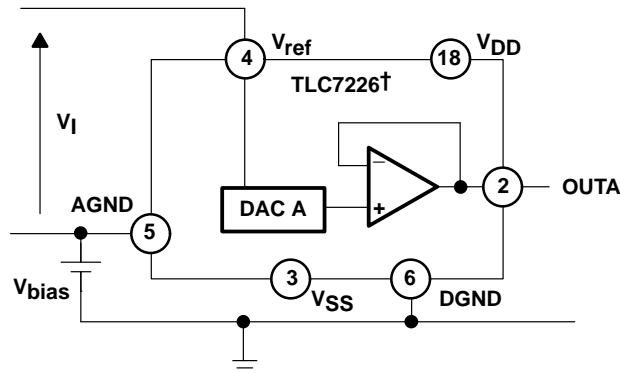
## AGND bias for positive output offset

The TLC7226 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset zero analog output voltage level. Figure 2 shows a circuit configuration to achieve this for channel A of the TLC7226. The output voltage,  $V_O$ , at OUTA can be expressed as:

$$V_O = V_{BIAS} + D_A (V_I)$$

Where  $D_A$  is a fractional representation of the digital input word ( $0 \leq D \leq 255/256$ ).

Increasing AGND above system GND reduces the output range.  $V_{DD} - V_{ref}$  must be at least 4 V to ensure specified operation. Because the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7226. Supply voltages  $V_{DD}$  and  $V_{SS}$  for the TLC7226 should be referenced to DGND.



† Digital inputs omitted for clarity.

Figure 2. AGND Bias Circuit

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## interface logic information

Address lines A0 and A1 select which DAC accepts data from the input port. The following function table shows the operations of the four DACs. Figure 3 shows the input control logic. When the  $\overline{WR}$  signal is low, the input latches of the selected DAC are transparent and the output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of  $\overline{WR}$ . While  $\overline{WR}$  is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

FUNCTION TABLE

CONTROL INPUTS			OPERATION
$\overline{WR}$	A1	A2	
H	X	X	No operation Device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = low, H = high, X = irrelevant

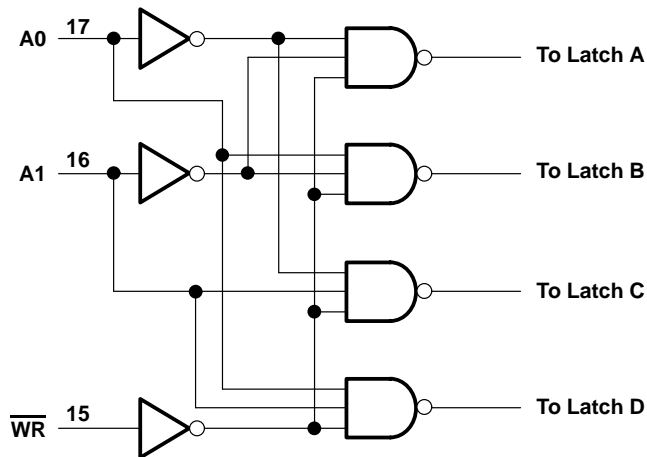


Figure 3. Input Control Logic

# TLC7226C, TLC7226I

## QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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### unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7226, with the output voltages having the same positive polarity as  $V_{ref}$ . The TLC7226 can be operated with a single supply ( $V_{SS} = AGND$ ) or with positive/negative supplies. The voltage at  $V_{ref}$  must never be negative with respect to AGND to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 4. Transfer values are shown in Table 2.

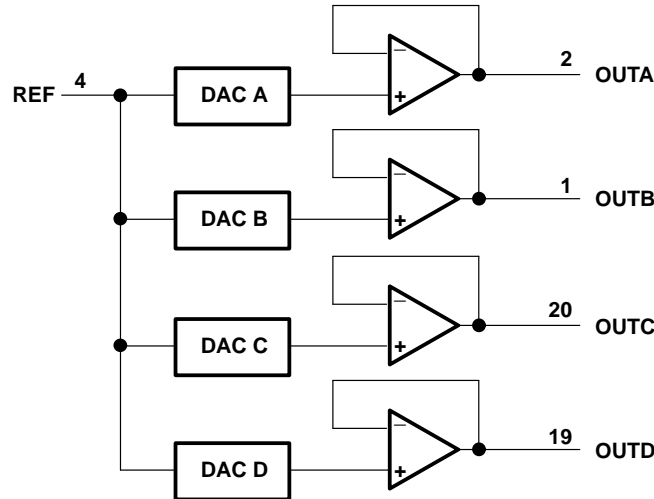


Figure 4. Unipolar Output Circuit

Table 2. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+ V_{ref} \left( \frac{255}{256} \right)$
1000	0001	$+ V_{ref} \left( \frac{129}{256} \right)$
1000	0000	$+ V_{ref} \left( \frac{128}{256} \right) = + \frac{V_{ref}}{2}$
0111	1111	$+ V_{ref} \left( \frac{127}{256} \right)$
0000	0001	$+ V_{ref} \left( \frac{1}{256} \right)$
0000	0000	0 V

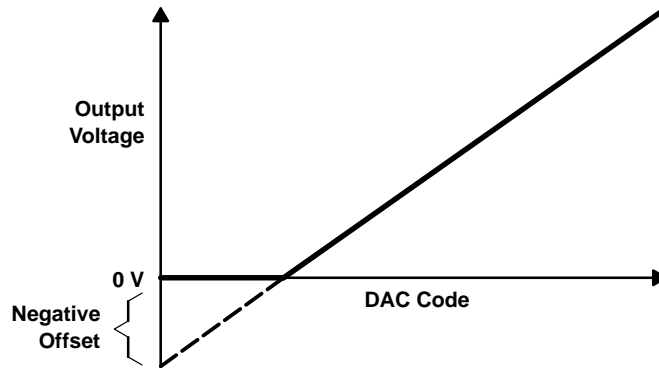
NOTE A.  $1 \text{ LSB} = (V_{ref} 2^{-8}) = V_{ref} \left( \frac{1}{256} \right)$

**linearity, offset, and gain error using single ended supplies**

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at zero volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in a transfer function shown in Figure 5.



**Figure 5. Effect of Negative Offset (Single Supply)**

This negative offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale is adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ : to AGND or DGND	.....	-0.3 V to 17 V
to $V_{SS}^\ddagger$	.....	-0.3 V to 24 V
Supply voltage range, $V_{SS}$ : to AGND or DGND	.....	-17 V to +0.3 V
Voltage range between AGND and DGND	.....	-17 V to 17 V
Input voltage range, $V_I$ (to DGND)	.....	-0.3 V to $V_{DD} + 0.3$ V
Reference voltage range: $V_{ref}$ (to AGND)	.....	-0.3 V to $V_{DD}$
$V_{ref}$ (to $V_{SS}$ )	.....	-0.3 V to 20 V
Output voltage range, $V_O$ (to AGND) (see Note 1)	.....	$V_{SS}$ to $V_{DD}$
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$ (see Note 2)	.....	500 mW
Operating free-air temperature range, $T_A$ : C suffix	.....	$0^\circ\text{C}$ to $70^\circ\text{C}$
I suffix	.....	$-25^\circ\text{C}$ to $85^\circ\text{C}$
Storage temperature range, $T_{stg}$	.....	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N packages	.....	$260^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The  $V_{SS}$  terminal is connected to the substrate and must be tied to the most negative supply voltage applied to the device.

- NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.  
2. For operation above  $T_A = 75^\circ\text{C}$ , derate linearly at the rate of 2 mW/ $^\circ\text{C}$ .

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$		4.5	16.5	V
Supply voltage, $V_{SS}$		-0.6	-5.5	V
High-level input voltage, $V_{IH}$	$V_{DD} = 4.75$ V	2		V
	$V_{DD} = 15.75$ V	2		
Low-level input voltage, $V_{IL}$	$V_{DD} = 4.75$ V		0.8	V
Reference voltage, $V_{ref}$		0	$V_{DD} - 4$	V
Load resistance, $R_L$		2		k $\Omega$
Setup time, address valid before $\overline{WR}$ , $t_{su(AW)}$ (see Figure 6)		0		ns
Setup time, data valid before $\overline{WR}$ , $t_{su(DW)}$ (see Figure 6)	$V_{DD} = 4.75$ V to 5.25 V	70		ns
	$V_{DD} = 4.75$ V to 5.25 V	180		
Hold time, address valid before $\overline{WR}$ , $t_{h(AW)}$ (see Figure 6)	$V_{DD} = 4.75$ V to 5.25 V	10		ns
	$V_{DD} = 4.75$ V to 5.25 V	20		
Hold time, data valid before $\overline{WR}$ , $t_{h(DW)}$ (see Figure 6)	$V_{DD} = 4.75$ V to 5.25 V	0		ns
	$V_{DD} = 4.75$ V to 5.25 V	20		
Pulse duration, $\overline{WR}$ low, $t_w$ (see Figure 6)	$V_{DD} = 4.75$ V to 5.25 V	50		ns
	$V_{DD} = 4.75$ V to 5.25 V	180		
Operating free-air temperature, $T_A$	C suffix	0	70	$^\circ\text{C}$
	I suffix	-25	85	$^\circ\text{C}$

# TLC7226C, TLC7226I

## QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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### electrical characteristics over recommended operating free-air temperature range

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_I$	Input current, digital	$V_I = 0\text{ V or }V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{DD}$	Supply current	$V_I = V_{IL}$ or $V_{IH}$ , $V_{DD} = 16.5\text{ V}$ , $V_{SS} = -5\text{ V}$ No load		6	16	mA
$I_{SS}$	Supply current	$V_I = V_{IL}$ or $V_{IH}$ , No load		4	10	mA
$r_{i(\text{ref})}$	Reference input resistance		2	4		$\text{k}\Omega$
	Power supply sensitivity	$\Delta V_{DD} = \pm 5\%$			0.01	%/%
$C_i$	Input capacitance	REF input	All 0s loaded	65		pF
			All 1s loaded		300	
		Digital inputs			8	



# TLC7226C, TLC7226I

## QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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### operating characteristics over recommended operating free-air temperature range

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			2.5			V• $\mu$ s
Settling time to 1/2 LSB	Positive full scale	$V_{ref} = 10$ V			5	$\mu$ s
	Negative full scale				7	
Resolution				8		Bits
Total unadjusted error		$V_{DD} = 15$ V $\pm 5\%$ , $V_{ref} = 10$ V			$\pm 2$	LSB
Linearity error	Differential/integral				$\pm 1$	LSB
Full-scale error		$V_{DD} = 15$ V $\pm 5\%$ , $V_{ref} = 10$ V			$\pm 2$	LSB
Gain error		$V_{DD} = 15$ V $\pm 5\%$ , $V_{ref} = 10$ V		$\pm 0.25$		LSB
Temperature coefficient of gain	Full scale	$V_{DD} = 14$ V to 16.5 V, $V_{ref} = 10$ V		$\pm 20$		ppm/ $^{\circ}$ C
	Zero-code error			$\pm 50$		$\mu$ V/ $^{\circ}$ C
Zero-code error				$\pm 20$	$\pm 80$	mV
Digital crosstalk glitch impulse area		$V_{ref} = 0$ V		50		nV•s

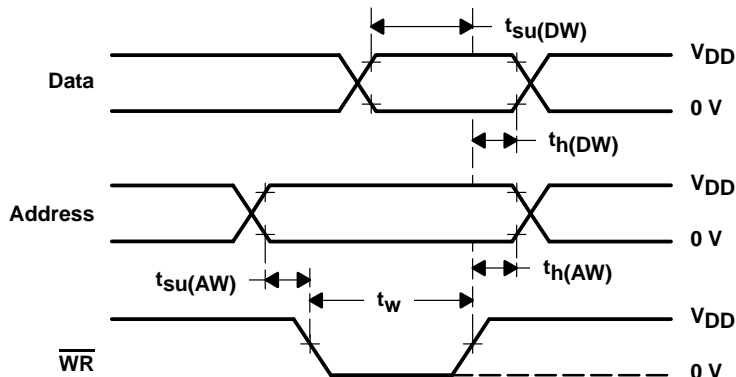
single power supply,  $V_{DD} = 14.25$  V to 15.75 V,  $V_{SS} = AGND = DGND = 0$  V,  $V_{ref} = 10$  V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, $I_{DD}$		$V_I = V_{IL}$ or $V_{IH}$ , No load			13	mA
Slew rate			2			V• $\mu$ s
Settling time to 1/2 LSB	Positive full scale				5	$\mu$ s
	Negative full scale				20	
Resolution				8		Bits
Total unadjusted error					$\pm 2$	LSB
Full-scale error					$\pm 1.5$	LSB
Temperature coefficient of gain	Full scale	$V_{DD} = 14$ V to 16.5 V, $V_{ref} = 10$ V		$\pm 20$		ppm/ $^{\circ}$ C
	Zero-code error			$\pm 50$		$\mu$ V/ $^{\circ}$ C
Linearity error	Differential				$\pm 1$	LSB
Digital crosstalk glitch impulse area				50		nV•s

single or dual power supplies,  $V_{DD} = 4.75$  V to 5.25 V,  $V_{SS} = AGND = DGND$  or  $V_{SS} = -5$  V,  $V_{ref} = 1.25$  V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, $I_{DD}$		$V_I = V_{IL}$ or $V_{IH}$ , No load		4	12	mA
Linearity error	Differential				$\pm 1$	LSB
Gain error					$\pm 4$	LSB
Zero-code error					$\pm 80$	mV

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $t_r = t_f = 20$  ns over  $V_{DD}$  range.  
 B. The timing measurement reference level is equal to  $V_{IH} + V_{IL}$  divided by 2.  
 C. The selected input latch is transparent while  $\overline{WR}$  is low. Invalid data during this time can cause erroneous outputs.

Figure 6. Write-Cycle Voltage Waveforms

TYPICAL CHARACTERISTICS

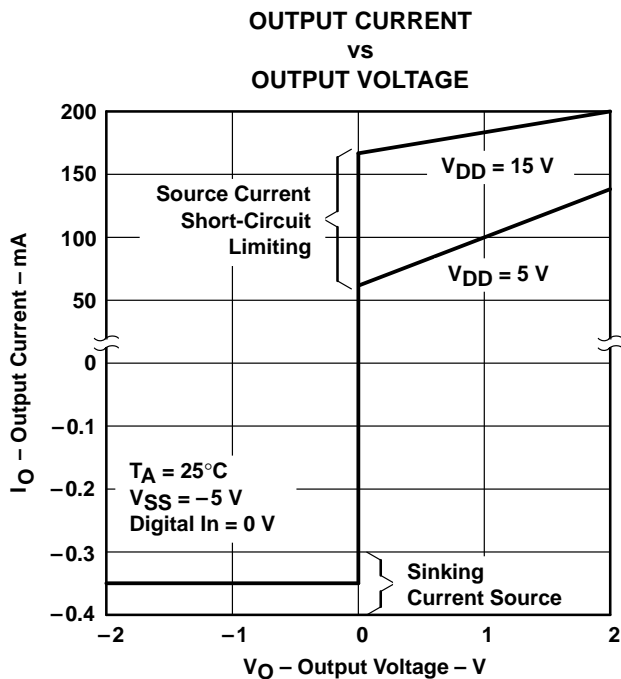


Figure 7

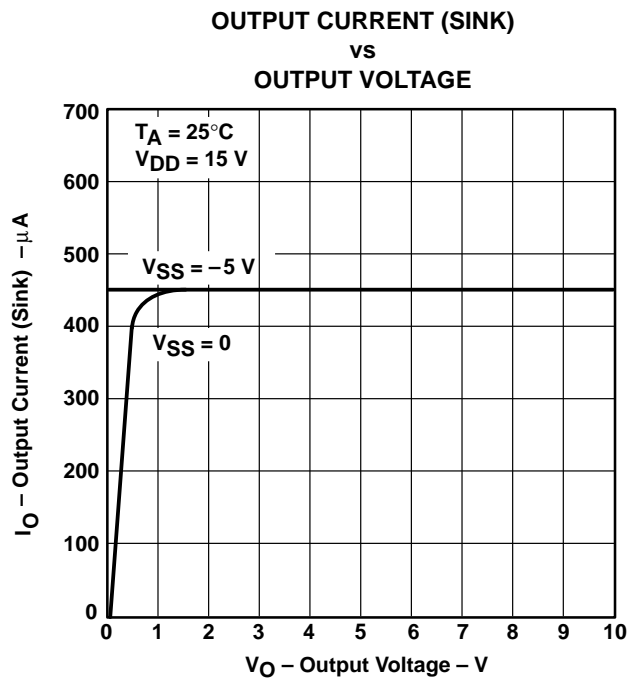


Figure 8

# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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## APPLICATION INFORMATION

### bipolar output operation using external amplifier

Each of the DACs of the TLC7226 can also be individually configured to provide bipolar output operation, using an external amplifier and two resistors per channel. Figure 9 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7226. In this case:

$$V_O = 1 + \frac{R_2}{R_1} \times (D_A \times V_{ref}) - \frac{R_2}{R_1} \times (V_{ref})$$

With  $R_1 = R_2$

$$V_O = (2D_A - 1) \times V_{ref}$$

Where  $D_A$  is a fractional representation of the digital word in latch A.

Mismatch between  $R_1$  and  $R_2$  causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7226 can be operated with a single supply or from positive and negative supplies.

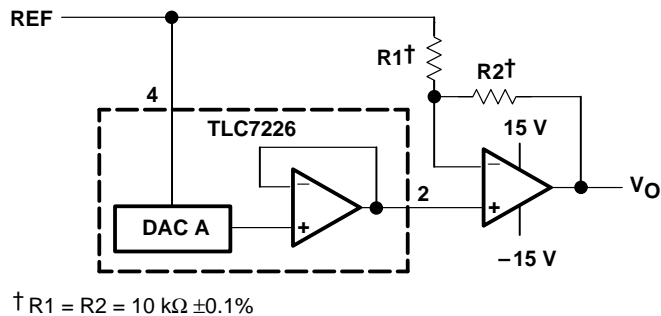


Figure 9. Bipolar Output Circuit

### staircase window comparator

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator shown in Figure 10 is a circuit that can be used to measure the  $V_{OH}$  and  $V_{OL}$  thresholds of a TTL device under test. Upper and lower limits on both  $V_{OH}$  and  $V_{OL}$  can be programmed using the TLC7226. Each adjacent pair of comparators forms a window of programmable size (see Figure 11). When the test voltage ( $V_{test}$ ) lines horizontal within a window, then the output for that window is higher. With a reference of 2.56 V applied to the REF input, the minimum window size is 10 mV.

APPLICATION INFORMATION

staircase window comparator (continued)

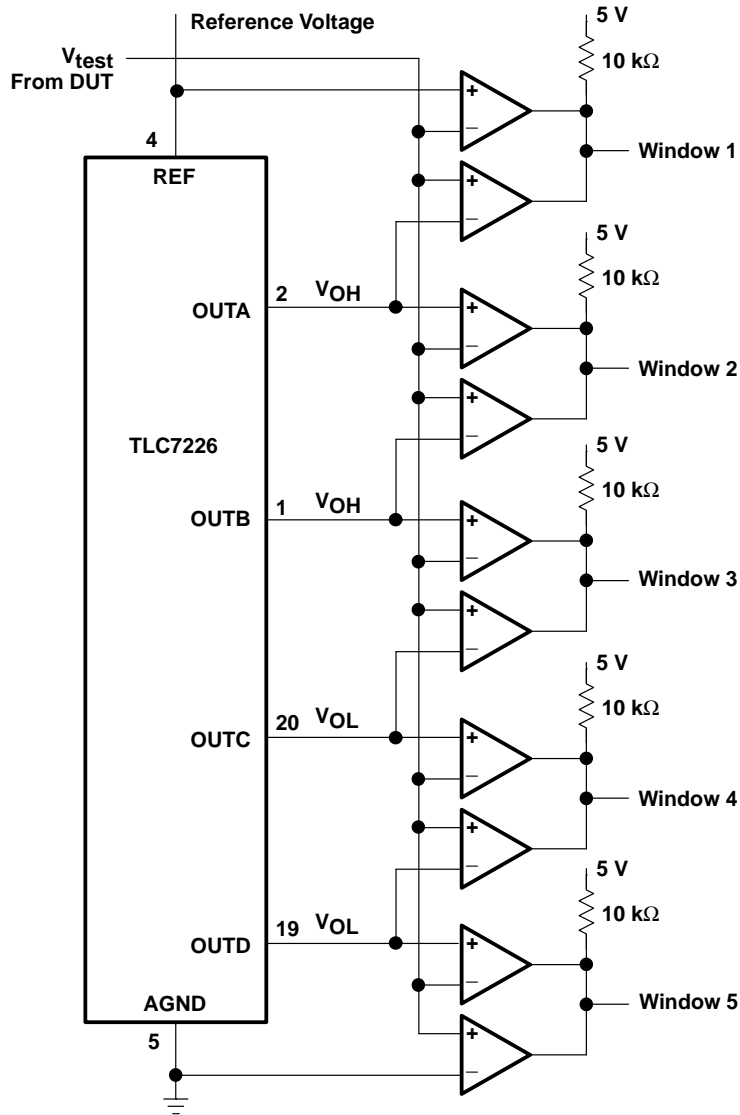


Figure 10. Logic Level Measurement

# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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## APPLICATION INFORMATION

### staircase window comparator (continued)

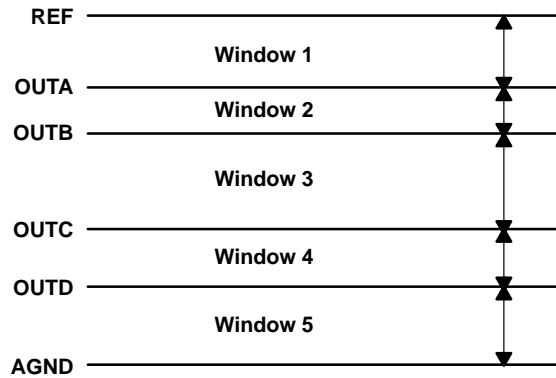


Figure 11. Window Structure

The circuit can easily be adapted as shown Figure 12 to allow for overlapping of windows. When the three outputs from this circuit are decoded, five different nonoverlapping programmable windows can again be defined (see Figure 13).

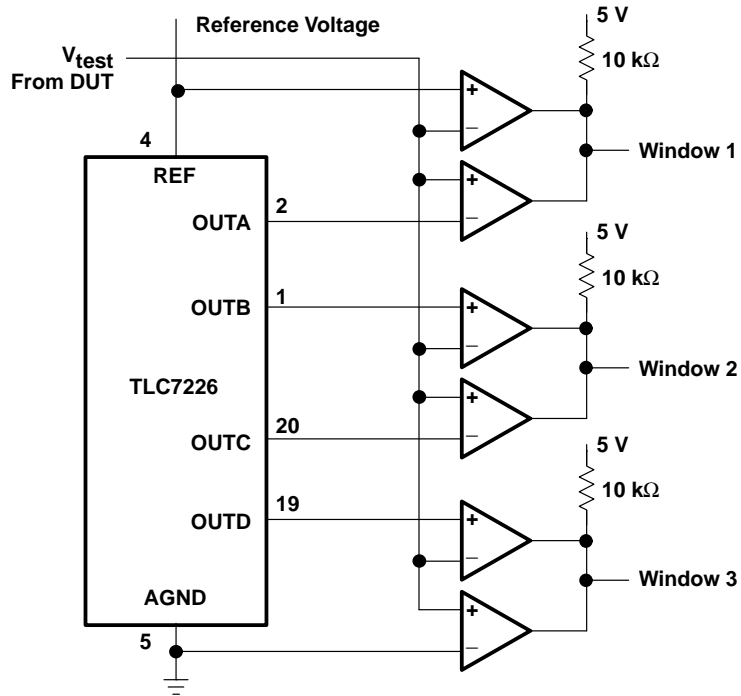


Figure 12. Overlapping Windows Circuit

APPLICATION INFORMATION

staircase window comparator (continued)

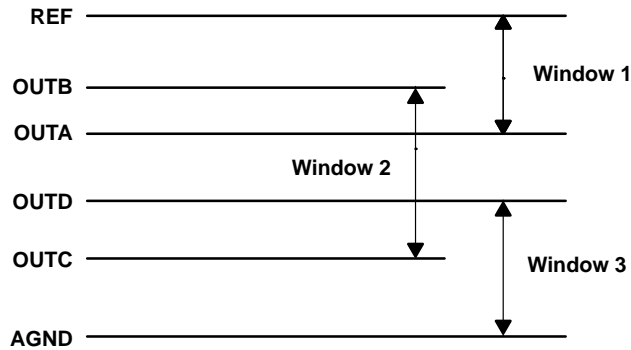


Figure 13. Window Structure

output buffer amplifier

The unity-gain output amplifier is capable of sourcing 5 mA into a 2-kΩ load and can drive a 3300-pF capacitor. The output can be shorted to AGND indefinitely or it can be shorted to any voltage between  $V_{SS}$  and  $V_{DD}$  consistent with the maximum device power dissipation.

multiplying DAC

The TLC7226 can be used as a multiplying DAC when the reference signal is maintained between 2 V and  $V_{DD} - 4$  V. When this configuration is used,  $V_{DD}$  should be 14.25 V to 15.75 V. A low output impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 14 shows the general schematic.

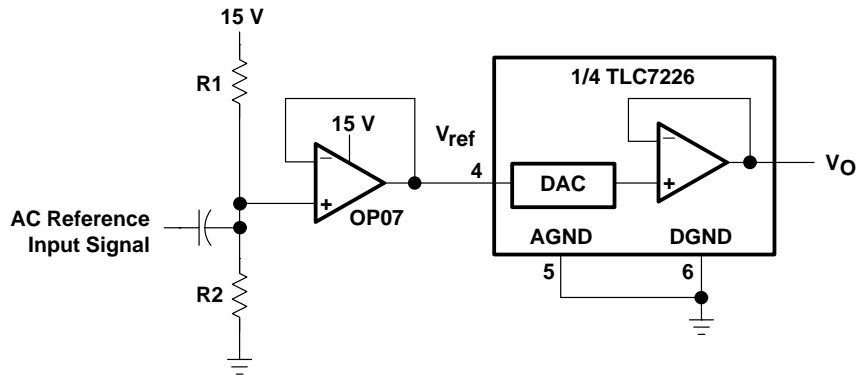


Figure 14. AC Signal Input Scheme

# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

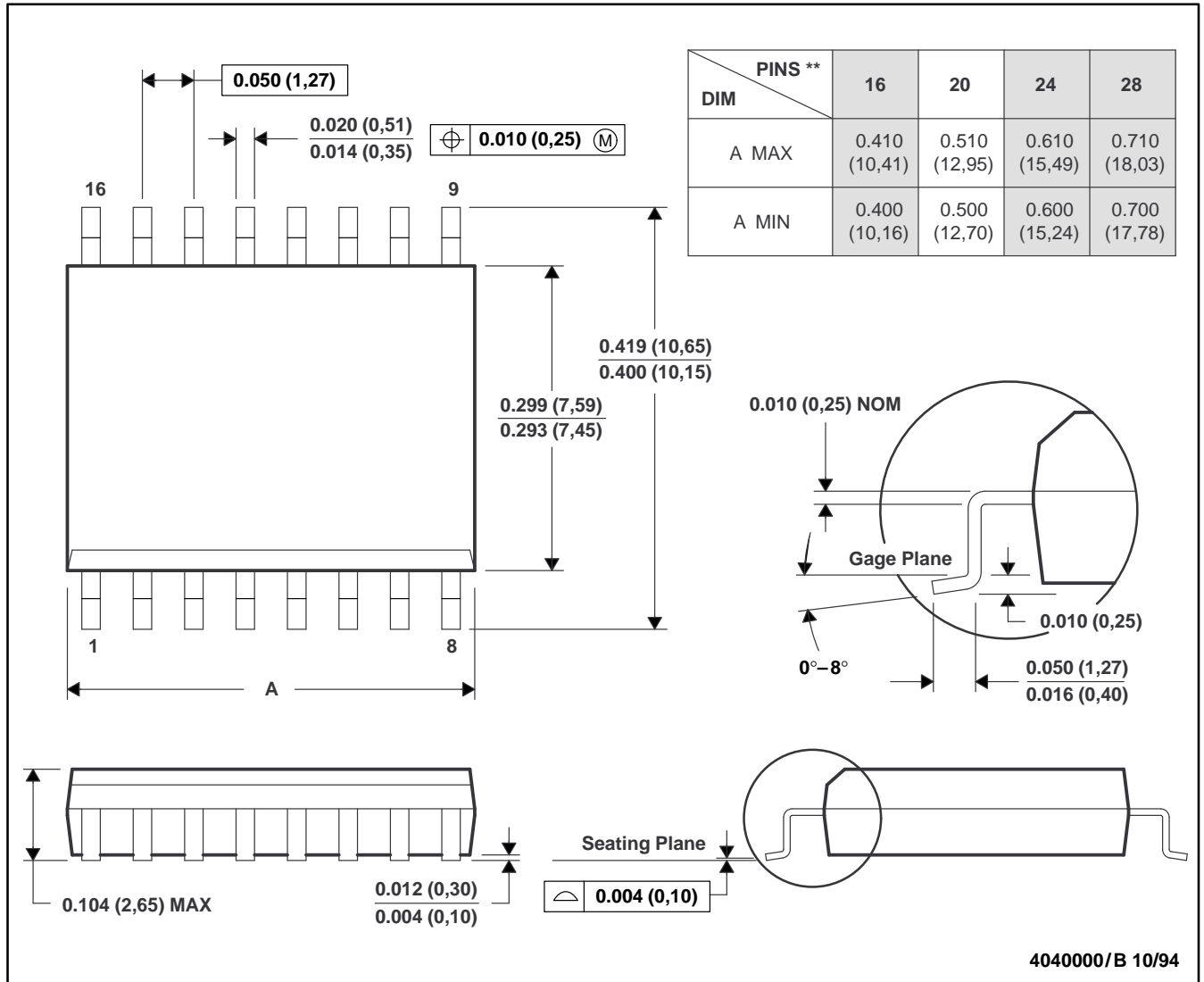
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## MECHANICAL DATA

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTE: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

# TLC7226C, TLC7226I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

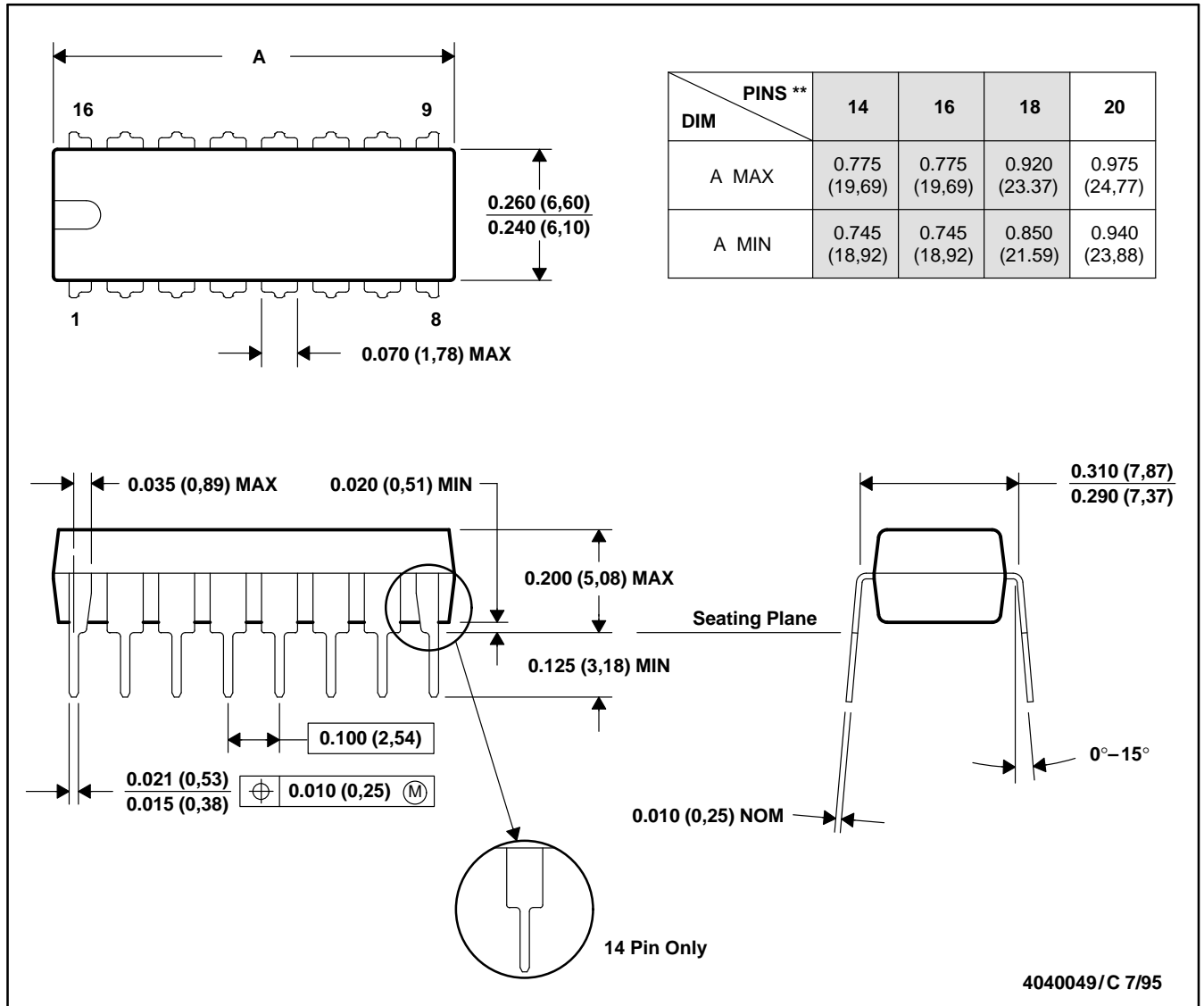
SLAS060A – JANUARY 1995 – REVISED DECEMBER 1995

## MECHANICAL DATA

**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)



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